IN THE CLAIMS

1-55. (Cancelled)

56. (Currently Amended) A system providing peripheral component device interconnection, comprising:

a peripheral device processor for controlling operation of the peripheral device; and

a host messaging unit, coupled to the peripheral device processor, but separate from the peripheral device processor, the host messaging unit retrieving host commands from a host memory of a host separate from the host messaging unit without the use of the processor of a peripheral device, validating the retrieved host commands and signaling to the host memory a successful asynchronous transfer of the host commands from host memory to the processor of the peripheral device;

wherein the host messaging unit comprises:

a read controller, coupled to the bus, for determining when the host commands have been provided to the host memory and for retrieving the host commands directly from the host memory via direct memory access asynchronous to the operation of the host processor and the peripheral device;

a write controller, coupled to the bus and to the read controller, the write controller clearing the host memory to allow the host to infer that the host command has been read by the host messaging unit;

a validator, coupled to the write controller and the read controller, the validator determining a validity of host commands retrieved from the host memory;

a read clock, coupled to the read controller, the read clock providing a signal for initiating reading of host commands from the host memory by the read controller; and

a busmaster command engine, coupled to the validator, read controller and bus, the busmaster command engine initiating the command retrieval from the host memory

when the busmaster command engine receives a signal from the ~~discrete~~ host indicating host commands are available in the host memory.

57. (Previously Presented) The system of claim 56, wherein the host messaging unit retrieves host commands from a host memory of the host without adding process loading to a host processor of the host.

58. (Previously Presented) The system of claim 56, wherein the host messaging unit provides signaling between the peripheral device and the discrete host asynchronous to operation of the host and the peripheral device.

59. (Previously Presented) The system of claim 56, wherein the host messaging unit is disposed external to the peripheral device and provides signaling between a plurality of processors of peripheral devices and the host, the operation of the host messaging unit being asynchronous to operation of the host and the processors of the peripheral devices.

60. (Canceled)

61. (Currently Amended) The system of claim [[60]] 56, wherein the busmaster command engine comprises a register programmable for indicating that the command is available to be retrieved from the host memory.

62. (Currently Amended) The system of claim [[60]] 56, wherein the read clock is programmable to allow predetermined retrieval intervals.

63. (Currently Amended) The system of claim [[60]] 56, wherein the read clock restarts the predetermined interval after the host commands are retrieved from the host memory.

64-68. (Canceled)